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09/933,786	08/20/2001	Sam B Sandbote	4800P008	6730

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EXAMINER	
KIM, KENNETH S	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/933,786
Filing Date: August 20, 2001
Appellant(s): SANDBOTE, SAM B

Joseph T. Grunkemeyer
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed July 18, 2005.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Prior Art of Record

5,222,225	GROVES	6-1993
4,149,263	PRIOSTE	4-1979
4,896,133	METHVIN ET AL	1-1990
2003/0056064	GSCHWIND ET AL	3-2003

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 2, 11, 12, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Groves, U.S. Patent No. 5,222,225, cited in the previous office action.

Groves teaches the invention substantially as claimed in claim 1 including an apparatus comprising:
(a) a shift-post processor (30).
(b) a shifter (22) to shift an operand according to an offset parameter (LSBS, starting address offset and XPCR, byte count) generating a shifted operand,
(c) a register (26) coupled to the shift post processor capable of transferring a shift carry operand stored in the register to the shift post processor, and coupled to the shifter to store the shifted operand (col. 7, line 38) after any transfer of the shift carry operand (col. 7, line 44),
(d) wherein the shift post processor coupled to the slitter and the register to process the shifted operand to generate an output based on at least a control signal (col. 3, line 56) and a mask field (col. 4, line 63),
(e) wherein the shift post processor (30) comprises a decoder to decode the offset parameter into mask field, the mask field having a plurality of mask bits, each of the mask bits corresponding to a byte position of the shifted operand (col. 4, line 67), and
(e) formatter coupled to the decoder to format the shifted operand using the control signal and the mask field (col. 4, line 65) – claim 2,

however, does not expressly state that the mask bits corresponding to bit positions (instead of byte position) of the operand are used.

It would have been obvious to a person of ordinary skill in the art that the method is applicable to any mask type including one that corresponds to bit positions, which represent the smallest unit (col. 1, line 27; col. 2, line 35). The person would have been motivated to use a mask corresponding to bit positions, when the shift desired is in units of bits instead of bytes.

The method claims 11 and 12 and the system claims 21 and 22 are equivalently rejected based on the same reason.

It is well known in the art that a bit mask with bits corresponding to each bit and a byte mask with bits corresponding to each byte are used in an equivalent setting.

Methvin et al (provided as an evidentiary reference) clearly shows application of a byte mask and a bit mask in an equivalent setting (col. 8, lines 53 - "a" and "A" differ by certain bits - and 57; col. 10, lines 57 and 59; col. 11, lines 30 and 32; col. 12, line 45; col. 16, line 51).

It is obvious to a person of ordinary skill in the art at the time the invention was made that the method and system of manipulating byte sequence of data using a byte mask is equally applicable to a method and system of manipulating bit sequence of data using a bit mask as the evidentiary reference demonstrated. Implementing a method and system using a bit mask when a method and system using a byte mask is known is within the realm of ordinary skill in the art.

Claims 3-10, 31, 13-20, 32, 23-30, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Groves, U.S. Patent No. 5,222,225 in view of Prioste, U.S. Patent No. 4,149,263, both cited in the previous office action.

Groves teaches the invention substantially as claimed as set forth in paragraphs above, however, does not expressly state that numeric data are bit shifted with sign and zero extension.

Prioste teaches a method of bit shifting numeric bit data with sign and zero extension (col. 4, line 11).

It would have been obvious to a person of ordinary skill in the art that the shifter and the shift post processor can be used for processing numeric bit data combined with sign and zero extension. The person would have been motivated to use the digital data processing method to process numeric data, as numeric data is a subset of digital data.

When numeric data bits are manipulated and shifted for realignment, sign or zero extension accompanies the manipulation, so that a valid numeric representation is obtained. It would have been obvious to a person of ordinary skill in the art that upon manipulation of numeric data bits using a bit mask performed in a similar manner as manipulation of bytes using a byte mask, one ought to provide sign and zero extension to obtain a valid numeric representation subsequent to the manipulation.

(10) Response to Argument

Applicant argued that the reference does not teach using mask bits each corresponding to a bit position of the shifted operand but instead teaches using mask bits each corresponding to byte positions of a shifted operand.

Applicant argued that there is no showing of a *prima facie* case of obviousness, because there is no suggestion or motivation to modify the reference and there is no reasonable expectation of success.

Examiner respectfully disagrees. Mask bits are used to selectively operate on data items regardless of the length of the item. Each mask bit is used for each item. One could use mask bits, which are made up of groups of identical mask bits each corresponding to each bit of a data item and each group corresponding to each data item, but that approach has not been in favor due to undesirable waste of resources.

When the length of a data item subject to a selective operation is one bit, mask bits each corresponding to each bit data item are used. On the other hand, when the length of a data item subject to a selective operation is one byte (eight bits), mask bits each corresponding to each byte data item are used. It is within the realm of an ordinary skill in the art to use mask bits each corresponding to each data item of any length of interest (as shown in the evidentiary references; Methvin et al; Gschwind et al, par. 67). It is obvious to one of ordinary skill who has knowledge of using mask bits each corresponding to each byte to use mask bits each corresponding to each bit with a reasonable expectation of success. (Examiner is not required to show the reasonable expectation of success.)

Applicant further argued that there is no motivation to combine bit unit operation of sign and zero extension with byte unit operation of shift and mask, since the combination produces no useful result.

Examiner's position is that, as data operations in bit units are obvious in light of data operations in byte units as applied to shift and mask operations, it is obvious to combine the bit unit operation of sign and zero extension with bit unit operations of shift and mask when the data operations are on items of numeric data (evidentiary support: Gschwind et al, par. 5, line 7). One would have been motivated to combine the operations to obtain a valid representation of a numeric value.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

KENNETH S. KIM
PRIMARY EXAMINER

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September 13, 2005

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